7 PROGRAMMABLE LOGIC CONTROLLERS BERNECKER-RAINER – HARDWARE, BASIC PROGRAMMING.

Study duration: 90 min.

7.1 Programmable logic controllers Bernecker Rainer

The controller generation B&R system 2000 is an automation system that sets new standards in performance, functionality and operational safety. The systems B&R 2003, B&R 2005 and B&R 2010 cover the entire application range from simple logic processors to complex, decentralized, divided, automation systems. Each system differs in structure, assembly, modularity and CPU performance. They are, however, so closely related that programmer compatibility is ensured and the basic objectives of fully centralized and decentralized compatibility are provided.

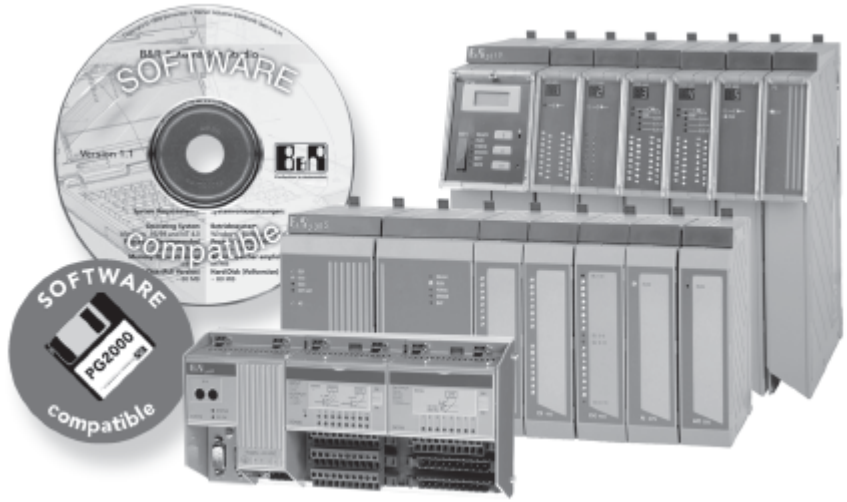


Fig. 7.1: Overview of B&R Systems.

7.1.1 System 2003

The B&R System 2003 can be used as both a complete control system as well as a remote I/O system for the expansion of industrial PCs and controllers from all B&R system families. Distributed systems can also be created. Many different interfaces for fieldbus systems and networks guarantee trouble-free communication. [36]

System 2003 central processing units cover a wide performance spectrum. The optimal price/performance ratio is achieved by fine-tuning processing power, memory capacity, integrated communication interfaces, and local slots for I/O screw-in modules. Clearly arranged diagnostic LEDs have been implemented to indicate the controller's status. Programming is achieved in a uniform manner using B&R Automation Studio™.

Fig. 7.2: Example of CP.

When using the System 2003 as a remote I/O system, bus controllers are available for CAN bus, ETHERNET Powerlink and X2X Link connection. Bus controllers handle the local peripherals and forward I/O signals via the network.

For the System 2003, B&R offers a large number of I/O modules in various designs. Analog values, digital signals, timers and counters allow many process variables to be handled and various actuators to be controlled.

Tab. 7.1: Overview of B&R 2003 modules and its basic characteristics.

Module	**Description**
CP 430	2003 CPU, 100KB SRAM, 256 KB Flash PROM, 24VDC, 7W supply, 1 RS232 interface, 1 CAN interface, CAN max. 64 digital/32 analog I/O points
CP 470	2003 CPU, 100KB SRAM, 256 KB Flash PROM, 24VDC, 14W supply, 1 RS232 interface, 1 CAN interface, CAN max. 128 digital/64 analog I/O points
CP 474	2003 CPU, 100KB SRAM, 512 KB Flash PROM, 24VDC, 12,6W supply, 1 RS232 interface, 1 CAN interface, CAN, 4 slots for screw in modules, max. 208 digital/80 analog I/O points
CP 476	2003 CPU, 750KB SRAM, 512 KB Flash PROM, 24VDC, 12,5W supply, 1 RS232 interface, 1 CAN interface, CAN, 4 slots for screw in modules, max. 272 digital/80 analog I/O points
CP 770	2003 CPU, 100KB SRAM, 512 KB Flash PROM, 100-240VAC, 14W supply, 1 RS232 interface, 1 CAN interface, CAN, 4 slots for screw in modules, max. 128 digital/64 analog I/O points
CP 774	2003 CPU, 100KB SRAM, 512 KB Flash PROM, 100-240VDC, 12,6W supply, 1 RS232 interface, 1 CAN interface, CAN, 4 slots for screw in modules, max. 208 digital/80 analog I/O points

The System 2003 allows flexible creation of remote I/O stations in a machine or system. A large number of network and fieldbus interfaces allow connection to the complete spectrum of B&R automation systems and many other systems as well. The large number of different screw-in modules provides connections for any sensor or actuator signal. Programming a remote system is no different than programming a centralized system.

The System 2003 is ideally suited for the distribution of machines and systems in self-sufficient units or cells with integrated intelligence. Line communication between the units takes place using standard Ethernet TCP/IP networks or fieldbus systems. In each unit, the System 2003 can be expanded with drives, operator panels or peripherals. The palette of CPUs allows the computing power to be matched to the requirements of the machine unit.

The System 2003 has much more to offer. The compact controller is also suited for large tasks. If the CPU with local I/O system is networked via ETHERNET Powerlink with the various decentralized components, a very powerful system is created for demanding tasks with highly dynamic movement processes.

7.1.2 System 2005

The System 2005 is the high-performance controller from B&R. Its large amount of bandwidth for the input and output of signals from peripherals covers all of the requirements of machine manufacturing, plant manufacturing, and process engineering. Together with I/O systems, industrial PCs, and controllers from B&R, automation solutions are created that meet the highest demands. Modern interfaces, together with fieldbus systems, networks, and peripheral devices, provide optimal data throughput.

The newest System 2005 CPUs are based on Intel-compatible processors with the most modern architecture. Innovative PC technology such as Compact Flash memory, Ethernet connections, and aPCI expansion slots allow the highest performance equipment from the IT world to be made available for automation. The performance palette is rounded off by proven CPUs with Motorola processors. Programming takes place in a completely compatible and uniform fashion using B&R Automation Studio™.

To reduce wiring, remote operation of System 2005 I/O modules is also possible. Bus controllers remove location limitations and bring the connection terminals closer to the machine. The data throughput of ETHERNET Powerlink also guarantees the highest performance for decentralized systems.

A wide range of modules for connecting analog, digital, counter, temperature, and other signals allows the System 2005 to control many process values and many different types of actuators. The parallel I/O processor reduces the load on the CPU and provides more power in the application. [36]

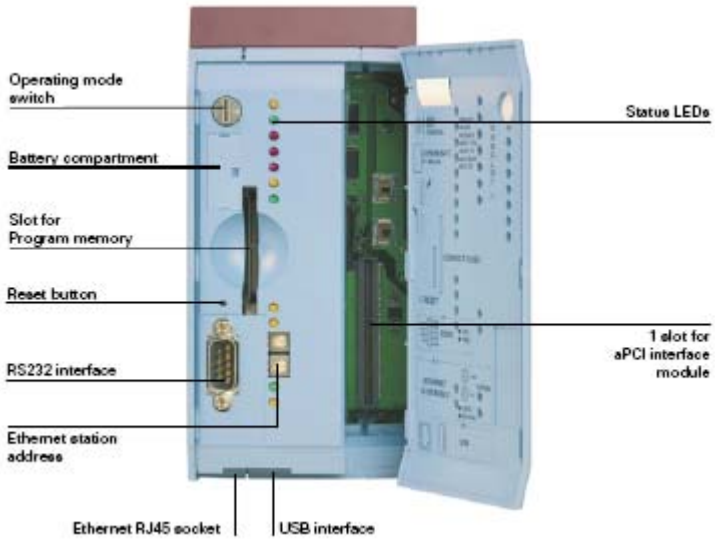


Fig. 7.3: Central processor unit CP360.

Tab. 7.2: Overview of B&R 2005 modules and its basic characteristics.

Module	Description
CP 260	2005 CPU, 4MB DRAM, 850 kB SRAM, 512 KB Flash PROM, 1 PCMCIA slot, 1 RS232
CP 340	2005 CPU, x86 233 Intel compatible, 16MB DRAM, 512KB SRAM, exchangeable Compact Flash, 1 slot pro aPCI modul, 1 USB interface, 1 RS232, 1 Ethernet 100Base
CP 360	2005 CPU, Pentium 266, 32MB DRAM, 512 SRAM, exchangeable Compact Flash, 1 slot pro aPCI, 1 USB interface, 1 RS232, 1 Ethernet 100 Base T
CP 380	2005 CPU, Pentium III 500, 64MB DRAM, 512 SRAM, exchangeable Compact Flash, 1 slot pro aPCI, 1 USB interface, 1 RS232, 1 Ethernet 100 Base T
CP 382	2005 CPU, Pentium III 500, 64MB DRAM, 512 SRAM, exchangeable Compact Flash, 3 slot pro aPCI, 1 USB interface, 1 RS232, 1 Ethernet 100 Base T

Communication with the outside world and a decentralized architecture are characteristics of modern automation products. The System 2005 has been optimized to meet these demands and offers high-performance interfaces with a wide bandwidth. Interface modules for networks and fieldbus systems expand the connections already integrated in the CPUs.

Remote I/O System

The System 2005 allows flexible creation of high-performance, remote I/O stations in a machine or system. A large number of network and fieldbus interfaces allow connection to the complete spectrum of B&R automation systems and many other systems as well. Programming a remote system is no different than programming a centralized system.

Systems 2005 I/O can be used centrally on the controller and in a remote switching cabinet. Networking with ETHERNET Powerlink also allows synchronization of all local and remote data points with a precision better than 1 µs. Drives are also connected together or with the controller with the same precision.

The System 2005, together with B&R I/O systems, drives and operator panels, are excellently suited for automation of large, complex machines and systems. Flexibility, expandability and scalable performance classes allow the most modern machine concepts to be realized. A real example from the packaging industry combines decentralized operation, 50 drives, and 50 remote I/O systems as well as more then 60 I/O modules with IP67 protection distributed throughout the machine room.

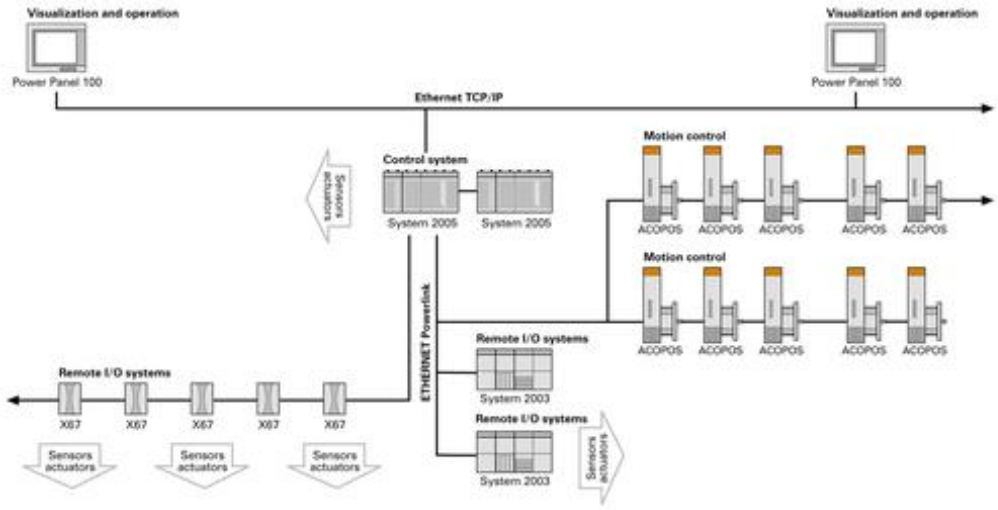


Fig. 7.4: Communication network with B&R System 2005.

7.1.3 System 2010

One prominent feature of the B&R 2010 control system is the separation of the **System and I/O Bus**. I/O and power supply modules are situated on the I/O bus and system modules plug into the system bus (e.g. network modules, multiprocessors).

The use of separate bus systems provides the following advantages:

- Higher data throughput, since the system and I/O buses do not affect each other:
  - The I/O-bus has a constant, deterministic and cyclic data responsibility for managing classic PCC modules (e.g. digital or analog input/output modules).
  - High volumes of data appear sporadically on the system bus, however due to the separate bus systems, the data stream on the I/O-bus is not disturbed.
- Secure I/O data transfer.

The module address of the 2010 expansion slave is set with a node number switch, from where the 2010 I/O module addresses begin. Settings are made in steps of ten (00, 10, ..., 90). A maximum of 20 I/O modules can be installed on one of these bus segments. However, it is possible to use up to 99 modules with a 2010 expansion master.

Fig. 7.5: System 2010.

7.2 Maximum number of expansion modules in B&R System 2003 and 2005

Each programmable logic controller has defined the maximum number of inputs and outputs. Each module in B&R system has a physical and logical address.

7.2.1 B&R System 2003

Physical module slots

A physical module slot corresponds to the actual space required for a module. 2003 modules can be single width (=one module slot) or double width (= two module slots), for example like the CP 474. Module racks are available in different lengths for the B&R System 2003. The palette ranges from one module slot to a maximum of 10 module slots (= module addresses or slots in the hardware view in Automation Studio)

Logical module slots

Some modules require more than one logica module slot. That means the numer of physical module slots required is different than the numer of logica modules slots required. The maximum numer of logica module slots depends on the controller. The controller also determines how many module slots are available for analog modules. Various controller are limited as to the maximum number of analog module slots and also as to the module slots for analog modules. Both conditions must be met.

Tab. 7.3: Maximum expansions inputs and outputs.

CPU	Maximum number of log. Module slots	Maximum number of analog module slots	Possible module addresses for analog modules
CP 430	4	2	1-4
CP 470/CP770	6	4	1-8
CP474/CP774	12	4	1-8
CP 476	16	4	1-8
EX 270	4	2	1-2
EX 470/	8	4	1-4

CPU	Maximum number of log. Module slots	Maximum number of analog module slots	Possible module addresses for analog modules
EX770			
EX 477/ EX777	6	4	1-6

The following table contains an overview of the modules that use more than two logica module slots or that an analog module slot.

If a module uses the logical module slots and one of these slots is an analog module slot, it is always the first one. The number of logical module slots corresponds to the module addresses used (=slots in the hardware view in Automation Studio).

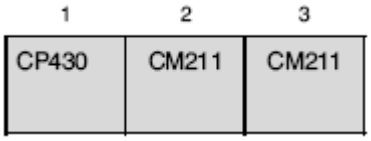
Tab. 7.4: Expansions modules and its numbering.

Module	Number of logical module slots	Number of analog module slots	Number of phys. module slots used
AF 101	1	1	1
DI 439	2	-	1
DM 465	2	-	1
CM 211	2	1	1
CM 411	2	2	1

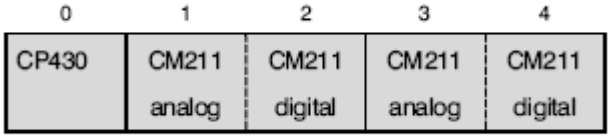
Example of hardware configuration

Configuration with one CP 430 and two CM211.

Physical module assignments (physical module slots)



Logical module assignments (module addresses)



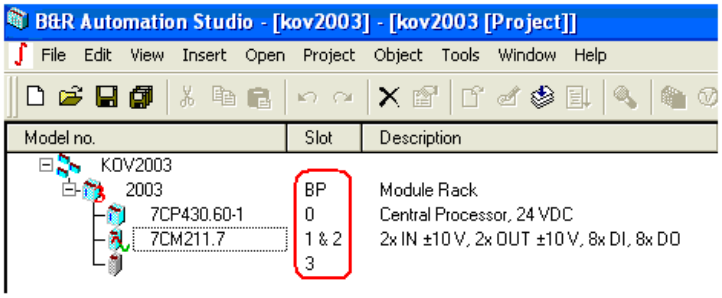


Fig. 7.6: Hardware configuration in the B&R Automation Studiu.

7.2.2 B&R system 2005

The following guidelines apply when configuring every B&R 2005 system:

- System modules are only allowed to be inserted on the main backplane.
- Empty slots must be filled with dummy modules.
- The **power supply** must always be located in the two furthest left slots (1 and 2) for both main and expansion backplanes.
- The **CPU** can be operated on the main backplane directly next to the power supply.
- Counting for **module addressing** begins at slot 3 which has address 1 on every backplane.

The module address is determined by the slot (slot coding). Module addressing begins with slot 3, which has address 1. For PLC systems with an operating system older than version 1.10, module addressing for system modules begins with address 0 (numbers are different for system modules and I/O modules).

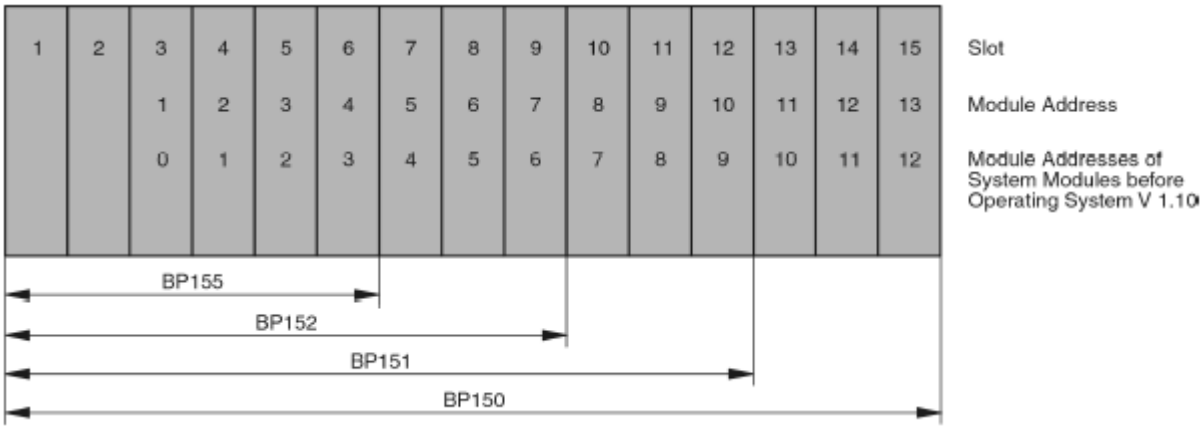


Fig. 7.7: Maximum expansion B&R System 2005 and its address in slots.

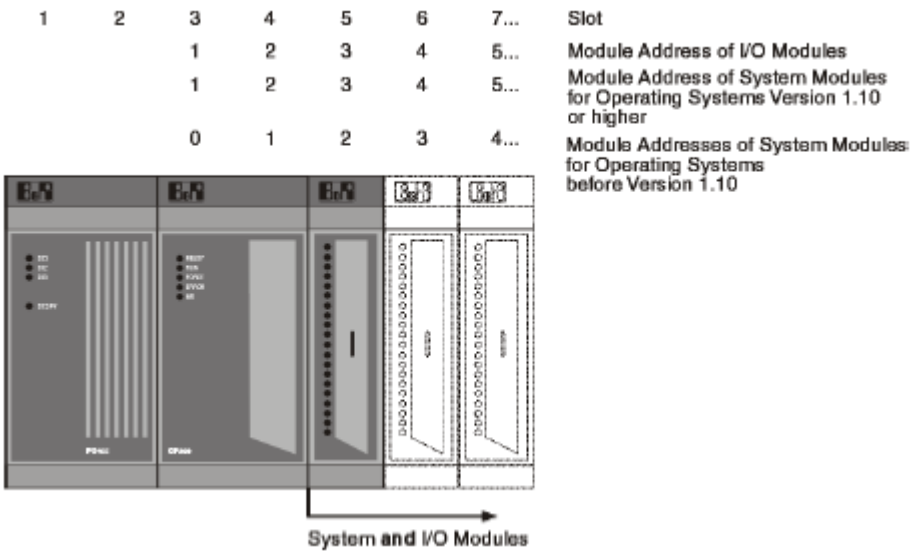


Fig. 7.8: B&R System 2005.

7.3 Generation programmable logic controller Bernecker-Rainer

The programmable logic controller Bernecker-Rainer (Bernecker Rainer uses the abbreviation PCC-programmable computer controller) are produced in two basic generation SG3 (System Generation 3) and SG4. The basic difference between the system generations are the used central processor units, because the system generation 3 is using CPU from the Motorola family and the system generation 4 is using CPU from the Intel family. [29]

System Generation 3 (SG3) - CPU of processors from the Motorola family.
The following CPUs belong to this series: CP260, IF260, IP161, XP152, IF100, IF101, CP100, CP104, CP152, CP153, CP200, CP210, CP430, CP470, CP474, CP476, CP770, CP774, PP21, PP41, PP15, LS251

System Generation 4 (SG4) - CPU of processors from the Intel family.
The following CPUs belong to this series: *PP1x0, PP2x0, CP380, CP382, CP360, AR102, AR105, AR010, AR000*

PCC with system generation 3

- B&R2000 systems with Motorola processors store data using the "Big Endian" format; i.e. A UDINT value places the highest significant byte in the lowest ordered address and the lowest significant byte in the highest ordered address.
- Uses cyclic and high speed task classes
- A large part of memory is automatically remanent, and all internal variables are remanent by default.
- FIX RAM is used to secure data during a cold restart.
- A cold restart is necessary for reconfiguring, reloading, etc., of various libraries and system modules.

Internally, warm restarts and cold restarts are completely different boot modes:

- A cold restart discards all data and reinitializes everything
- A warm restart holds on to all remanent data including remanent system structures, etc. and only checks consistency (checksums).
- On all CPUs, Flash memory is available for saving modules. That allows modules in Flash memory to be accessed directly (or code executed directly) on most CPUs. Deleted module memory is not available until the complete Flash memory is cleared. While saving modules in Flash, the interrupt is temporarily blocked, the module saved, the pending time interrupts acknowledged (so that no cycle time violations are reported) and then the cyclic system proceeds normally again. The application is therefore blocked while saving the module.
- Library functions are managed by the ADT (Address Distribution Table) which must be configured to the number of available entries. If too few entries exist, a failure is reported and adding a library is not carried out
- All SG3 CPUs have a hardware (HW) watchdog accessible cyclically by the Automation Runtime. In the event of an error (endless loop in an interrupt handler i.e. in the HS TC), the HW watchdog triggers a HW reset and reboots the system in Service mode (as with a PLC halt). In the error logbook, error 9210 (watchdog reboot or HW reset) is registered.
- The system manager is centrally important. It is the highest priority pSOS task and has to assign task class scheduling. This includes cycle time monitoring, cyclic checksum controlling, key handling and cyclic servers (SYS_service).

PCC with system generation 4

- Stores data in the "Little Endian" format, i.e. A UDINT value places the lowest significant byte in the lowest ordered address and the highest significant byte in the highest ordered address.
- Can only use cyclic task classes with desired cycle times, as well as smaller 10 msec. cycle. This way, all task classes have automatic uniform properties (scheduling, IO handling, cycle time monitoring, priority, etc.).
- "Main memory" (DRAM) is not remanent. Remanent memory (SRAM) is only available when additional modules are added (LS172, LS191, etc.) Accessing SRAM is much slower than accessing DRAM. Powerfail NMI logic does not exist on some AR systems (AR102, AR105, AR000) to guarantee that the contents of fast DRAM can be secured in the slower SRAM before a power failure. **For all these reasons, internal variables in AR are not remanent by default.**
  Remanent variables must be explicitly declared and stored in a physically separated memory area (SRAM).
- Cold restarts are not necessary since initialization occurs with a warm restart. No data has to be saved in FIX RAM to be protected (during the cold restart). The data are stored in UserRAM instead of FIX RAM.
- Warm restarts and cold restarts only differentiate themselves in the handling of remanent data. All remanent data (remanent variables, UserRAM) are deleted during a cold restart; a warm restart keeps them. In this way, only a warm restart is needed after saving a new SYSCONF module. Internally, AR systems do not find it necessary anymore to execute a **cold restart** (Exception: after **deleting the Flash ROM (UserROM)**, a cold restart is **STRONGLY recommended** since the remanent data

should also be deleted in the entire project.To hold on to remanent data as long as possible, AR executes a warm restart after a Diagnostics boot. In this way, data that would have been deleted by a cold restart is retained.

- B&R modules are stored in **File** form **on the hard disk** (compact-Flash) and a **copy in DRAM** (SysROM, UserROM) is also saved. Access to the module (data, code) always takes place using the faster DRAM. **The memory area of a deleted module is available right away** using the file system even without deleting the memory. Module saving takes place using normal file access without holding up the cyclic system.
- A flexible library manager replaces the ADT. The entries in this manager are stored dynamically and the number of entries does not have to be configured. The manager stores names with up to 32 significant characters. Additionally, the library name can be stored in order to enable differentiated name spaces in the future (the management of differentiated name spaces is not used yet. Names should be clear.)
- Only the CP360 uses a HW watchdog. With the other models (AR010, AR102, AR105 and AR000), only SW monitoring exists, i.e. task class cycle time monitor. In this way, an endless loop in an interrupt handler can lead to a halt of the system. Unlike SG3, AR applications are not run in an interrupt context. All task classes are normal OS tasks with lower priority than the central scheduler. In this way, an endless loop in an application cannot lead to a halt of the system. However, an error in Automation Runtime (base system + libraries with interrupt handling) can lead to this problem.
- The system manager is just a task with relatively higher priority which controls checksums and cyclic services (SYS_service) every 10 msec. For this reason, AR cancelled the controlling of "system cycle tolerance" (error code 6002).

7.4 Operating mode PCC

Tab. 7.5: Operating modes PCC.

Mode	Description
RUN	After booting, all software modules to be executed are copied to DRAM and started. The controller runs, i.e.all programs are executed. Beforehand, the syste was started with the configured boot cause (usually warm restart).
SERVICE	After biotiny, the task vlase system is not started. All activities can be carried out, as in RUN mode.
DIAGNOSTICS	This oeprationg state only allows modules to be deleted from the target system, the logbook to be read, memory to be deleted, adn a cold/warm restart to be carried out. Only modules from System ROM are loaded. Memory can only be erased in diagnostics mode.
BOOT	Allows an operating system download to be executed. Compact Flash can be formatted and partitioned.

7.5 Memory of PLC

Working with memory is very important and is a decisive factor when creating professional application software. A solid knowledge of the basics is extremely useful when working with memory in the form of variables, arrays, structures, pointers and freely allocated memory areas, in order to have a clear overview of the entire application.

When programming, it is important to assign values to various variables, therefore various standard types have been defined for the variables. [26]

Different storage media can be used on the automation targets. They can be roughly divided into RAM and ROM. Sections of each of these memory areas are available to the user while others are exclusively reserved for the operating system and cannot be used by the user.

- RAM: RAM is a high-speed read/write memory which mostly contains the data for executing programs. Data stored here is only kept as long as the memory is provided with power. It's divided into the following:
  - DRAM: DRAM is RAM memory that can be used to store software objects, variable values, tables, etc. It is distinguished by its high-speed access. This type of memory is not battery-backed, which means that all data is lost in the event of a power failure.
  - SRAM: Also called static RAM. Unlike DRAM, SRAM is battery-backed. Data is maintained as long as the buffer is working properly.
- ROM: ROM memory is slow and is used for long-term storage of data. The data is also maintained even in the absence of power supply. Flash (Compact Flash) is a typical type of ROM memory. The operating system and the application are stored here.

Remanent or permanent variables should be used only when absolutely necessary. There are other ways to store data securely, e.g. data objects or files.

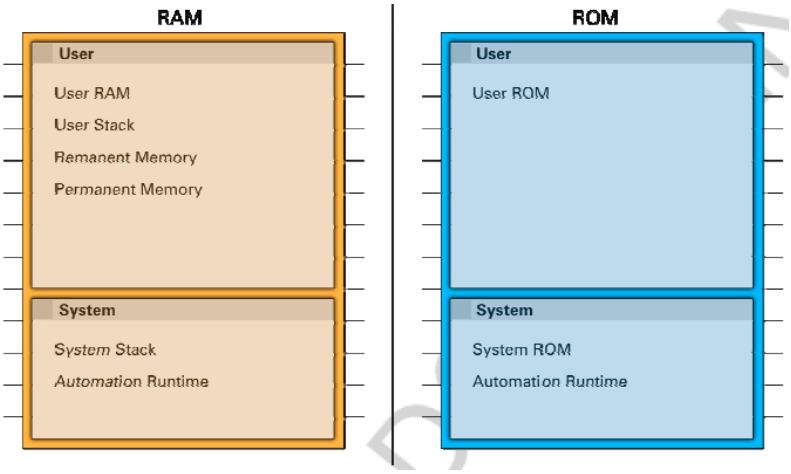


Fig. 7.9: Memory structure.

When the system is running, all data is stored on DRAM because of its faster access time. In this case, the SRAM serves as storage medium for remanent data and data objects. Remanent data is the data which must be stored when power is not being supplied or when the system is restarted.

SYSROM and USRROM are located on the Compact Flash when power is not on. The memory areas REMMEM (remanent data) and USRRAM are located on the SRAM. During booting, the BR objects from the SYSROM and USRROM memory areas are copied into DRAM. REMMEM memory is copied to DRAM in exactly the same way. USRRAM memory is not copied since the amount of time during a power failure is not sufficient to also secure this memory.

During a power failure, remanent data from the DRAM is backed up on the SRAM within a limited time frame. When a power failure is detected, data that should be remanent is backed up in

the SRAM. However, this NMI logic (power failure logic) is not provided on all systems.

The corresponding user documentation should state whether the selected system is equipped with NMI logic.

Memory Allocation

When programming software, just creating arrays or arrays from structures is often not sufficient because these can only be defined with a fixed dimension during the time before being compiled.

It is not possible to create arrays or arrays from structures with more than 4095 array elements. Furthermore, very large arrays will cause the maximum variable memory for each task or the global variable memory in the project, which is limited to 32 Kbytes on SG3 and 64Kbytes on SG4 systems, to be filled up very quickly.

In this case, it makes sense to create a memory area dimensioned according to the conditions once the system is running. Use dynamic access of this memory to manage it with the help of offset calculations. As a result, the software will be somewhat more complex, but also more dynamic an configurable than when using static array variables.

Questions:

1. *What is the difference between a PLC from B&R2003 and a PLC from B&R2005?*
2. *What is the difference between a PLC from B&R2005 and a PLC from B&R2010?*
3. *Do you explain individual operating modesPLC?*
4. *How is the memory divided?*
5. *How are the differences between system generation 3 (SG3) and system generation 4 (SG4)?*
6. *If you would like to store a file to compact flash you will use system generation 3 or system generation 4?*